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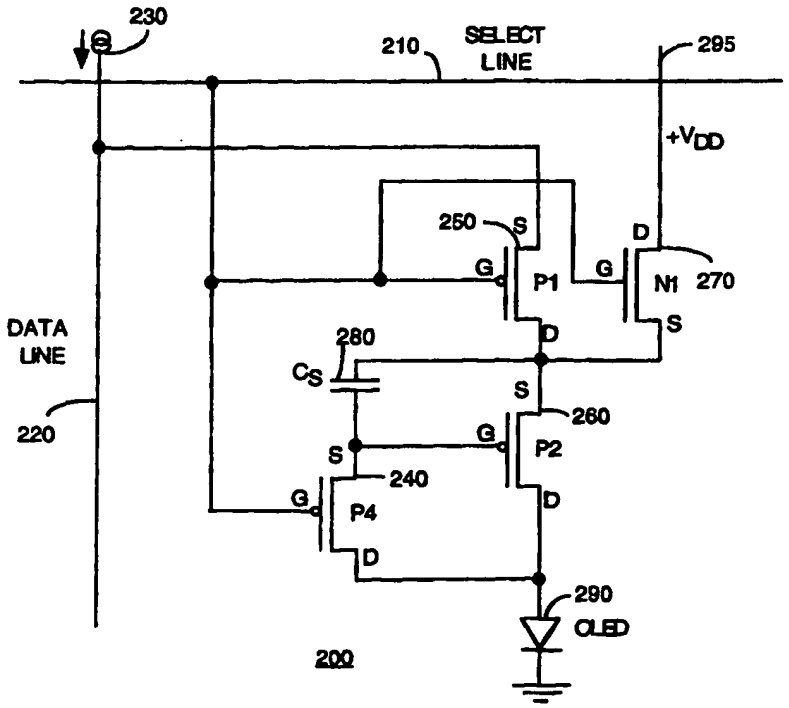
(57) Abstract

A LED pixel structure (200, 300, 400, 600, 700) that reduces current nonuformities and threshold voltage variations in a "drive transistor" of the pixel structure is disclosed. The LED pixel structure incorporates a current source for loading data into the pixel via a data line. Alternatively, an auto zero voltage is determined for the drive transistor prior to the loading of data.



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ACTVE MATRIX LIGHT EMITTING DIODE PIXEL STRUCTURE AND METHOD

This application claims the benefit of U.S. Provisional Application No. 60/ 044, 174 filed April 23, 1997, which is herein incorporated by reference.

This invention was made with U.S. government support under contract number F33615-96-2-1944. The U.S. government has certain rights in this invention.

The invention relates to an active matrix light emitting diode pixel structure. More particularly, the invention relates to a pixel structure that reduces current nonuniformities and threshold voltage variations in a "drive transistor" of the pixel structure and method of operating said active matrix light emitting diode pixel structure.

BACKGROUND OF THE DISCLOSURE

Matrix displays are well known in the art, where pixels are illuminated using matrix addressing as illustrated in FIG. 1. A typical display 100 comprises a plurality of picture or display elements (pixels) 160 that are arranged in rows and columns. The display incorporates a column data generator 110 and a row select generator 120. In operation, each row is sequentially activated via row line 130, where the corresponding pixels are activated using the corresponding column lines 140. In a passive matrix display, each row of pixels is illuminated sequentially one by one, whereas in an active matrix display, each row of pixels is first loaded with data sequentially.

With the proliferation in the use of portable displays, e.g., in a laptop computer, various display technologies have been employed, e.g., liquid crystal display (LCD) and light-emitting diode (LED) display. An important distinction between these two technologies is that a LED is an emissive device which has power efficiency advantage over non-emissive devices such as (LCD). In a LCD, a fluorescent backlight is on for the entire duration in which the display is in use, thereby dissipating power

even for "off" pixels. In contrast, a LED (or OLED) display only illuminates those pixels that are activated, thereby conserving power by not having to illuminate "off" pixels.

Although a display that employs an OLED pixel structure can reduce power consumption, such pixel structure may exhibit nonuniformity in intensity, which is attributable to two sources, threshold voltage drift of the drive transistor and transistor nonuniformity due to manufacturing. However, it has been observed that the brightness of the OLED is proportional to the current passing through the OLED.

Therefore, a need exists in the art for a pixel structure and concomitant method that reduces current nonuniformities and threshold voltage variations in a "drive transistor" of the pixel structure.

SUMMARY OF THE INVENTION

In one embodiment of the present invention, a current source is incorporated in a LED (OLED) pixel structure that reduces current nonuniformities and threshold voltage variations in a "drive transistor" of the pixel structure. The current source is coupled to the data line, where a constant current is initially programmed and then captured.

In an alternate embodiment, the constant current is achieved by initially applying a reference voltage in an auto-zero phase that determines and stores an auto zero voltage. The auto zero voltage effectively accounts for the threshold voltage of the drive transistor. Next, a data voltage which is referenced to the same reference voltage is now applied to illuminate the pixel.

In an another alternate embodiment, a resistor is incorporated in a LED (OLED) pixel structure to desensitize the dependence of the current passing through the OLED to the threshold voltage of the drive transistor.

BRIEF DESCRIPTION OF THE DRAWINGS

The teachings of the present invention can be readily understood by considering the following detailed description in conjunction with the accompanying drawings, in which:

FIG. 1 depicts a block diagram of a matrix addressing interface;

FIG. 2 depicts a schematic diagram of an active matrix LED pixel structure of the present invention;

FIG. 3 depicts a schematic diagram of an alternate embodiment of the present active matrix LED pixel structure;

FIG. 4 depicts a schematic diagram of another alternate embodiment of the present active matrix LED pixel structure;

FIG. 5 depicts a block diagram of a system employing a display having a plurality of active matrix LED pixel structures of the present invention;

FIG. 6 depicts a schematic diagram of an alternate embodiment of the active matrix LED pixel structure of FIG. 2; and

FIG. 7 depicts a schematic diagram of an alternate embodiment of an active matrix LED pixel structure of the present invention.

To facilitate understanding, identical reference numerals have been used, where possible, to designate identical elements that are common to the figures.

DETAILED DESCRIPTION

FIG. 2 depicts a schematic diagram of an active matrix LED pixel structure 200 of the present invention. In the preferred embodiment, the active matrix LED pixel structure is implemented using thin film transistors (TFTs), e.g., transistors manufactured using amorphous or poly-silicon. Similarly, in the preferred embodiment, the active matrix LED pixel structure incorporates an organic light-emitting diode (OLED). Although the present pixel structure is implemented using thin film transistors and an organic light-emitting diode, it should be understood that the present invention can be implemented using other types of transistors and light emitting diodes. For example, if transistors that are manufactured using other materials exhibit the threshold nonuniformity as discussed above, then the present invention can be employed to provide a constant current through the lighting element.

Although the present invention is illustrated below as a single pixel or pixel structure, it should be understood that the pixel can be employed with other pixels, e.g., in an array, to form a display. Furthermore,

although the figures below illustrate specific transistor configuration, it should be understood that the source of a transistor is relative to the voltage sign.

Referring to FIG. 2, pixel structure 200 comprises three PMOS transistors 240, 250, 260, a NMOS transistor 270, a capacitor 280 and a LED (OLED) 290 (light element). A select line 210 is coupled to the gate of transistors 240, 250 and 270. A data line is coupled to the source of transistor 250 and a $+V_{DD}$ line is coupled to the drain of transistor 270. One electrode of the OLED 290 is coupled to the drain of transistors 240 and 260. The source of transistor 240 is coupled to the gate of transistor 260 and to one terminal of capacitor 280. Finally, the drain of transistor 250, the source of transistor 270, the source of transistor 260 and one terminal of the capacitor 280 are all coupled together.

The present pixel structure 200 provides a uniform current drive in the presence of a large threshold voltage (V_t) nonuniformity. In other words, it is desirable to maintain a uniform current across the OLED, thereby ensuring uniformity in the intensity of the display.

More specifically, the OLED pixel structure is operated in two phases, a load data phase and a continuous illuminating phase.

Load Data Phase:

A pixel structure 200 can be loaded with data by activating the proper select line 210. Namely, when the select line is set to "Low", transistor P4 (240) is turned "On", where the voltage on the anode side of the OLED 290 is transmitted to the gate of the transistor P2 (260). Concurrently, transistor P1 (250) is also turned "ON" so that the constant current from the data line 220 flows through both the transistor P2 (260) and the OLED 290. Namely, the transistor 260 must turn on to sink the current that is being driven by the current source 230. The current source 230 that drives the data line is programmed by external data. The gate to source voltage of transistor 260 (drive transistor) will then settle to a voltage that is necessary to drive the current. Concurrently, transistor N1 (270) is turned "Off", thereby disconnecting the power supply $+V_{DD}$ from the OLED 290. The constant current source 230 will also self-adjust the

source-to-gate voltage to accommodate a fixed overdrive value (voltage) for transistor 260 and will compensate the threshold variation on the polysilicon TFT 260. The overdrive voltage is representative of the data. In turn, the data is properly stored on the storage capacitor Cs 280. This completes the load or write cycle for the data.

Continuous Illuminating Phase:

When the select line is set "High", both transistors of P1 (250) and P4 (240)are turned "Off" and the transistor N1 (270) is turned "On". Although the source voltage of the transistor 260 may vary slightly, the source-to-gate voltage of the transistor 260 controls the current level during the illumination cycle. The Vsg of transistor 270 across the capacitor 280 cannot change instantaneously. Thus, the gate voltage on transistor 260 will track with its source voltage such that the source-to-gate voltage is maintained the same throughout the entire Load and Illumination phases. The leakage current of polysilicon TFT and voltage resolution required for gray scale luminance of OLED will determine the size of storage capacitor needed for holding a valid data for a frame time. In the preferred embodiment, the capacitor is on the order of approximately .25 pf. Namely, the capacitor must be large enough to account for the current leakage of transistor 260. This completes the pixel operation for the illumination phase.

It should be noted that each data/column line 220 has its own programmed constant current source 230. During the illumination phase, the subsequent programmed current source on the data lines feeds through and loads the next rows of all pixels, while the pixels of previous rows are operating in the illumination phase for the whole frame time. Thus, this pixel structure of FIG. 2 requires only 3 PMOS transistors and 1 NMOS transistor with 2.5 lines. (select line, data line-current source and VDD voltage supply which can be shared with adjacent pixels).

Alternatively, FIG. 6 illustrates an implementation where the pixel structure of FIG. 2 is implemented with all PMOS transistors, which will provide economy for using either PMOS or NMOS processes only. The

NMOS transistor N1 is replaced with a PMOS P3 transistor 610. However, an additional line (control line) 620 is coupled to the gate of transistor 610 for addressing the additional PMOS transistor, thereby requiring a total of 3.5 lines, i.e., an additional voltage supply for controlling the additional PMOS gate.

In sum, the pixel structures of FIG. 2 and FIG. 6 are designed to compensate the threshold variation of both polysilicon TFT and the OLED by self-adjusting/tracking mechanism on Vsg of transistor 260 and by supplying a constant current source through the OLED 290. In fact, the pixel structures of FIG. 2 and FIG. 6 are able to accomplish proper operation during both Load and Illumination phases with hard voltage supply. These pixel structures can be implemented to design high-quality OLED displays with good gray scale uniformity and high lifetime despite instabilities in either the OLED or the pixel polysilicon TFT.

FIG. 3 illustrates an alternate embodiment of the present active matrix pixel structure. In this alternate embodiment, the data line voltage is converted into a current within the pixel structure without the need of a voltage-to-current converter such as the implementation of a current source as discussed above in FIGs. 2 and 6.

Referring to FIG. 3, pixel structure 300 comprises four PMOS transistors (360, 365, 370, 375) , two capacitors 350 and 355 and a LED (OLED) 380. A select line 320 is coupled to the gate of transistor 360. A data line 310 is coupled to the source of transistor 360 and a $+V_{DD}$ line is coupled to the source of transistor 365 and one terminal of capacitor 355. An auto-zero line 330 is coupled to the gate of transistor 370 and an illuminate line is coupled to the gate of transistor 375. One electrode of the OLED 280 is coupled to the drain of transistor 375. The source of transistor 375 is coupled to the drain of transistors 365 and 370. The drain of transistor 360 is coupled to one terminal of capacitor 350. Finally, the gate of transistor 365, the source of transistor 370, one terminal of the capacitor 350 and one terminal of the capacitor 355 are all coupled together.

More specifically, FIG. 3 illustrates a pixel structure 300 that is operated in three phases: 1) an auto-zero phase, 2) a load data phase and 3) an illuminating phase.

Auto-Zero:

When auto-zero line 330 and the illuminate line 340 are set to "Low", transistor P2 (375)and P3 (370) are turned "On" and the voltage on the drain side of transistor P1 (365) is transmitted to the gate and is temporarily connected as a diode. The data line 310 is set to a "reference voltage" and the select line 320 is set to "Low". The reference voltage can be arbitrarily set, but it must be greater than the highest data voltage.

Next, the illuminate line 340 is set to "High", so that transistor P2 375 is turned "Off". The pixel circuit now settles to a threshold of the transistor P1 365 (drive transistor), thereby storing a voltage (an auto-zero voltage) that is the difference between the reference voltage on the data line and the threshold voltage of the transistor P1 365 on the capacitor C_c 350. This sets the gate voltage, or more accurately V_{SG} of transistor 365 to the threshold voltage of transistor 365. This, in turn, will provide a fixed overdrive voltage on transistor P1 (365) regardless of its threshold voltage variation. Finally, Auto Zero line 330 is set to "High", which isolates the gate of transistor P1 365. The purpose of auto-zero is henceforth accomplished.

Load Data Phase:

At the end of the Auto Zero phase, the select line was set "Low" and the data line was at a "reference voltage". Now, the data line 310 is set to a data voltage. This data voltage is transmitted through capacitor C_C 350 onto the gate of transistor P1 (365). Next, the select line is set "High". Thus, the V_{SG} of transistor 365 provides transistor 365 with a fixed overdrive voltage for providing a constant current level. This completes the load data phase and the pixel is for illumination.

Continuously Illuminating Data Phase During Deselect Row Phase:

With the data voltage stored on the gate of transistor P1 (365), the illuminate line 340 is set to "Low", thereby turning "On" transistor P2 375. The current supplied by the transistor P1 365, is allowed to flow through

the OLED 380. In sum, the transistor 365 behaves like a constant current source. This completes the Illumination phase.

FIG. 4 illustrates another alternate embodiment of the present active matrix pixel structure. In this alternate embodiment, the data line voltage is also converted into a current within the pixel structure without the need of a voltage-to-current converter such as the implementation of a current source as discussed above in FIGs. 2, and 6.

Referring to FIG. 4, pixel structure 400 comprises three PMOS transistors (445, 460, 465) , two capacitors 450 and 455 and a LED (OLED) 470. A select line 420 is coupled to the gate of transistor 445. A data line 410 is coupled to the source of transistor 445 and a VSWP line is coupled to the source of transistor 460 and one terminal of capacitor 455. An auto-zero line 430 is coupled to the gate of transistor 465. One electrode of the OLED 470 is coupled to the drain of transistors 465 and 460. The drain of transistor 445 is coupled to one terminal of capacitor 450. Finally, the gate of transistor 460, the source of transistor 465, one terminal of the capacitor 450 and one terminal of the capacitor 455 are all coupled together.

More specifically, FIG. 4 illustrates a pixel structure 400 that is also operated in three phases: 1) an auto-zero phase, 2) a load data phase and 3) an illuminating phase.

Auto-Zero (By VSWP) Phase:

VSWP (voltage switching supply) is set to a "lower voltage" by the amount "ΔV", where the lower voltage is selected such that the OLED 470 is trickling a small amount of current (depending on the OLED characteristic, e.g., on the order of nanoamp). The lower voltage is coupled through onto the gate of transistor P1 (460) $V_{G(P1)}$ without dilution due to the floating node between the transistor P4 (445) and C_C (450) coupling capacitor. When Auto Zero line 430 is then set to "Low", the transistor P1 (460) (drive transistor) is temporarily connected as a diode by closing the transistor P3 (465). The select line 420 is then set to "Low" and a "reference voltage" is applied on the data line 410. The reference voltage can be arbitrarily set, but it must be greater than the highest data voltage.

The pixel circuit is now allowed to settle to the threshold of transistor P1 460. Finally, Auto Zero line 430 is then set to "High", which isolates the gate of transistor P1 460. The effect of this Auto Zero phase is to store on the capacitor C_c 450 a voltage (an auto-zero voltage) that represents the difference between the reference voltage on the data line and the transistor threshold voltage of P1 460. This completes the auto-zero phase.

Load Data Phase:

At the end of the Auto Zero phase, the select line was set "Low" and the data line was at a "reference voltage". Next, the data line is then switched from a reference voltage to a lower voltage (data voltage) where the change in the data is referenced to the data. In turn, the data voltage (data input) is load coupled through capacitors 450 and 455 to the gate of transistor P1 460. The voltage V_{SG} of the transistor 460 provides the transistor P1 (460) with a fixed overdrive voltage to drive the current for the OLED 470. Namely, the data voltage will be translated into an overdrive voltage on transistor P1 460. Since the voltage stored on the capacitor 450 accounts for the threshold voltage of the transistor P1 460, the overall overdrive voltage is now independent of the threshold voltage of the transistor P1. The select line 420 is then set "High". This completes the load data phase.

Continuously Illuminate Data During Deselect Row Phase:

At the completion of the data loading phase, the gate of transistor P1 460 is now isolated except for its capacitive connections, where the overdrive voltage for driving the OLED is stored on capacitor C_s 455. Next, the VSWP is returned to its original higher voltage (illuminate voltage). In turn, with VSWP rising, there is now sufficient voltage to drive the OLED for illumination. Namely, when select line 420 is set to "High", both transistors P3 (465) and P4 (445) are turned "Off", and the data voltage is kept in storage on V_{SG} of transistor 460 as before. This source-to-gate voltage $V_{SG(P1)}$ is maintained in the same manner throughout the entire Illumination phase, which means the current level through the OLED will be constant. This completes the Illumination cycle.

In sum, FIG. 3 discloses a pixel structure that uses 4 PMOS transistors and 1 coupling capacitor with 3 $^1/_2$ lines. (Auto-Zero line and VDDH voltage supply can both be shared). FIG. 4 discloses a pixel structure that uses only 3 PMOS transistors and 1 coupling capacitor with $2^1/_2$ line. (VSWP switching power supply could be share with adjacent pixel) Both of these two pixel structures can compensate the threshold variation of both polysilicon TFT and OLED by illuminating and auto-zero trickling current mechanism on $V_{SG(P1)}$. The aforementioned two (2) pixel structures can also be implemented in polysilicon NMOS and in amorphous NMOS design.

The two (2) pixel structures of FIG. 3 and FIG. 4 can be implemented to design high-quality OLED with good gray scale uniformity and high lifetime despite instabilities in either the OLED or the pixel polysilicon TFT.

FIG. 7 depicts a schematic diagram of an active matrix LED pixel structure 700 of the present invention. In the preferred embodiment, the active matrix LED pixel structure is implemented using thin film transistors (TFTs), e.g., transistors manufactured using poly-silicon or amorphous silicon. Similarly, in the preferred embodiment, the active matrix LED pixel structure incorporates an organic light-emitting diode (OLED). Although the present pixel structure is implemented using thin film transistors and an organic light-emitting diode, it should be understood that the present invention can be implemented using other types of transistors and light emitting diodes.

The present pixel structure 700 provides a uniform current drive in the presence of a large threshold voltage (V_t) nonuniformity. In other words, it is desirable to maintain a uniform current through the OLEDs, thereby ensuring uniformity in the intensity of the display.

Referring to FIG. 7, pixel structure 700 comprises two PMOS transistors 710 and 720, a capacitor 730, a resistor 750 and a LED (OLED) 740 (light element). A select line 770 is coupled to the gate of transistor 710. A data line 760 is coupled to the source of transistor 710. One terminal of resistor 750 is coupled to the source of transistor 720 and one electrode of the OLED 740 is coupled to the drain of transistor 720. Finally, the drain of

transistor 710, the gate of transistor 720 and one terminal of the capacitor 730 are all coupled together.

More specifically, when a row containing a pixel structure is selected to be the active row, a logical "high" level on the select line 770 turns on transistor M1 710, thereby allowing capacitor C 730 to be charged to a voltage V_g from the data line 760. After this row is deselected by a "low" level on the select line 770, which turns transistor M1 off, the voltage on the capacitor 730 is stored for the frame time. Since this voltage appears on the gate of transistor M2 720, it sets a current through transistor 720 that also passes through the OLED 740, which is located in the drain of the transistor 720.

More importantly, a resistor 750 is implemented in the present pixel structure. The resistor is coupled to the source of transistor 720 and serves as a negative feedback element. If an individual drive transistor has an unusually low threshold voltage, the transistor tends to pass more current to the OLED, but the additional current causes an additional voltage drop across the resistor 750, thereby reducing the current.

A complementary effect occurs with a drive transistor having an unusually high threshold voltage. The overall effect is to reduce the nonuniformity in the current. It has been observed that resistors can be generally formed with much better resistance uniformity than the threshold voltage uniformity achieved with TFTs. One reason is that TFT threshold voltages are very sensitive to the trap density in the active silicon material, whereas the resistance of the doped layers used in resistors is much less sensitive to trap density. Measurements have shown that the percentage variation of resistance is very small across a polysilicon display wafer, and to the extent that resistance does vary, it is expected to be smoothly varying, unlike transistor thresholds.

The current passing through the OLED 740 determines its brightness. However, it has been observed that when the pixel is implemented using TFTs, the threshold voltages of the TFTs can also vary over life as discussed above. In addition, there can be initial nonuniformities in the TFT threshold voltages. It should be noted that such nonuniformity with regard to transistor 710 is not a problem, since

its threshold voltage does not have a strong effect on the current that is established through the OLED. In contrast, variations in the threshold voltage of drive transistor 720 directly affect the current through the OLED.

More specifically, the current, I_{OLED} passing through the OLED in the present pixel structure can be expressed as:

$$I_{OLED} = \frac{K'}{2}\frac{W}{L}(V_g - V_t - I_{OLED}R)^2 \quad (1)$$

where K' is the intrinsic transconductance parameter of the transistor M2, W and L are its width and length, V_t is its threshold voltage, V_g is the voltage from the data line, and resistor R 750 has a value of 1M in the preferred embodiment. However, the resistor value may range from 100K to 10M depending on the drive transistor characteristics. It has been observed that the present pixel structure may reduce the current variation to 1/3 of what is possible without the present resistor as discussed below.

More specifically, it can be shown that with a resistor coupled to the source of transistor 720, the normalized sensitivity of the current through the diode to threshold voltage variations $\frac{1}{I_{OLED}} \frac{dI_{OLED}}{dV_t}$ is:

$$-2/(V_g - V_t + I_{OLED} R). \quad (2)$$

It is beneficial to increase the gate voltage V_g as much as possible, but with the limitation that the transistor 720 must stay in saturation. By introducing a voltage drop across the resistor (I_{OLED} R), the sensitivity to threshold voltage variations can be reduced below what would be achievable without a resistor. Ultimately, the term (I_{OLED} R) cannot become larger than ($V_g - V_t$), since such result would imply that transistor 720 was turned off. Therefore, the maximum reduction in sensitivity that can be achieved by placing a resistor in the source of transistor 720 is a factor of 2.

However, placing a resistor in the source permits the transistor 720 width W to be increased, where such increase reduces standard deviation of the threshold voltage, σ_{V_t}. For a fixed maximum gate voltage, W can be increased, thereby deriving more benefit from the statistical reduction in σ_{V_t}. Thus, by putting a resistor in the source of the transistor 720, a reduction in current variation can be achieved through the combined effect of (1) reducing the sensitivity to threshold variations $\frac{1}{I_{OLED}} \frac{dI_{OLED}}{dV_t}$ (limited to a theoretical maximum benefit of 2X, or 50% reduction), and (2) reducing the threshold variation σ_{V_t} itself (no limit except for geometrical and capacitance constraints).

FIG. 5 illustrates a block diagram of a system 500 employing a display 520 having a plurality of active matrix LED pixel structures 200, 300, 400, 600 or 700 of the present invention. The system 500 comprises a display controller 510 and a display 520.

More specifically, the display controller can be implemented as a general purpose computer having a central processing unit CPU 512, a memory 514 and a plurality of I/O devices 416 (e.g., a mouse, a keyboard, storage devices, e.g., magnetic and optical drives, a modem and the like). Software instructions for activating the display 520 can be loaded into the memory 514 and executed by the CPU 512.

The display 520 comprises a pixel interface 522 and a plurality of pixels (pixel structures 200, 300, 400, 600 or 700). The pixel interface 522 contains the necessary circuitry to drive the pixels 200, 300, 400, 600 or 700. For example, the pixel interface 522 can be a matrix addressing interface as illustrated in FIG. 1.

Thus, the system 500 can be implemented as a laptop computer. Alternatively, the display controller 510 can be implemented in other manners such as a microcontroller or application specific integrated circuit (ASIC) or a combination of hardware and software instructions. In sum, the system 500 can be implemented within a larger system that incorporates a display of the present invention.

Although the present invention is described using PMOS transistors, it should be understood that the present invention can be

implemented using NMOS transistors, where the relevant voltages are reversed. Namely, the OLED is now coupled to the source of the NMOS drive transistor. By flipping the OLED, the cathode of the OLED should be made with a transparent material.

Although various embodiments which incorporate the teachings of the present invention have been shown and described in detail herein, those skilled in the art can readily devise many other varied embodiments that still incorporate these teachings.

What is claimed is:

1. A display (520) comprising a plurality of pixels, each pixel (200) comprising:

a first transistor (250) having a gate, a source and a drain, where said gate is coupled to a select line (210), where said source is coupled to a data line (220);

a second transistor (270) having a gate, a source and a drain, where said gate of said second transistor is coupled to said select line, where said drain of said second transistor is coupled to a V_{DD} line (295), where said source of said second transistor is coupled to said drain of said first transistor;

a third transistor (240) having a gate, a source and a drain, where said gate of said third transistor is coupled to said select line;

a capacitor (280) having a first terminal and a second terminal, where said source of said third transistor is coupled to said first terminal of said capacitor, where said second terminal of said capacitor is coupled to said drain of said first transistor;

a fourth transistor (260) having a gate, a source and a drain, where said source of said fourth transistor is coupled to said drain of said first transistor, where said gate of said fourth transistor is coupled said source of said third transistor; and

a light element (290) having two terminals, where said drain of said fourth transistor and said drain of said third transistor are coupled to one of said terminal of said light element.

2. The display of claim 1, further comprising:

a current source (230) for coupling to said data line.

3. A display (520) comprising a plurality of pixels, each pixel (600) comprising:

a first transistor (250) having a gate, a source and a drain, where said gate is coupled to a select line (210), where said source is coupled to a data line (220);

a second transistor (610) having a gate, a source and a drain, where said gate of said second transistor is coupled to a control line (620), where said source of said second transistor is coupled to a V_{DD} line (295), where said drain of said second transistor is coupled to said drain of said first transistor;

a third transistor (240) having a gate, a source and a drain, where said gate of said third transistor is coupled to said select line;

a capacitor (280) having a first terminal and a second terminal, where said source of said third transistor is coupled to said first terminal of said capacitor, where said second terminal of said capacitor is coupled to said drain of said first transistor;

a fourth transistor (260) having a gate, a source and a drain, where said source of said fourth transistor is coupled to said drain of said first transistor, where said gate of said fourth transistor is coupled said source of said third transistor; and

a light element (290) having two terminals, where said drain of said fourth transistor and said drain of said third transistor are coupled to one of said terminal of said light element.

4. A method of illuminating a display having a plurality of pixels, where each pixel contains a circuit for controlling application of energy to a light element, where said circuit comprises a drive transistor, said method comprising the steps of:

(a) loading data onto said pixel by applying a current on a data line,

(b) storing said data on a capacitor that is coupled to the drive transistor; and

(c) illuminating said light element in accordance with said stored data.

5. The method of claim 4, wherein said current is provided by a current source.

6. A display (520) comprising a plurality of pixels, each pixel (300) comprising:

a first transistor (360) having a gate, a source and a drain, where said gate is coupled to a select line (320), where said source is coupled to a data line (310);

a first capacitor (350) having a first terminal and a second terminal, where said drain of said first transistor is coupled to said first terminal of said first capacitor;

a second transistor (365) having a gate, a source and a drain, where said source of said second transistor is coupled to a V_{DD} line (390), where said gate of said second transistor is coupled to said second terminal of said first capacitor;

a second capacitor (355) having a first terminal and a second terminal, where said gate of said second transistor is coupled to said first terminal of said second capacitor, where said source of said second transistor is coupled to said second terminal of said second capacitor;

a third transistor (370) having a gate, a source and a drain, where said gate of said third transistor is coupled to an auto-zero line (330), where said source of said third transistor is coupled to said gate of said second transistor, where said drain of said third transistor is coupled to said drain of said second transistor;

a fourth transistor (375) having a gate, a source and a drain, where said gate of said fourth transistor is coupled to an illuminate line (340), where said source of said fourth transistor is coupled to said drain of said third transistor; and

a light element (380) having two terminals, where said drain of said fourth transistor is coupled to one of said terminal of said light element.

7. A display (520) comprising a plurality of pixels, each pixel (400) comprising:

a first transistor (445) having a gate, a source and a drain, where said gate is coupled to a select line (420), where said source is coupled to a data line (410);

a first capacitor (450) having a first terminal and a second terminal, where said drain of said first transistor is coupled to said first terminal of said first capacitor;

a second transistor (460) having a gate, a source and a drain, where said source of said second transistor is coupled to a VSWP line (440), where said gate of said second transistor is coupled to said second terminal of said first capacitor;

a second capacitor (455) having a first terminal and a second terminal, where said gate of said second transistor is coupled to said first terminal of said second capacitor, where said source of said second transistor is coupled to said second terminal of said second capacitor;

a third transistor (465) having a gate, a source and a drain, where said gate of said third transistor is coupled to an auto-zero line (430), where said source of said third transistor is coupled to said gate of said second transistor, where said drain of said third transistor is coupled to said drain of said second transistor; and

a light element (470) having two terminals, where said drain of said second transistor is coupled to one of said terminal of said light element.

8. A method of illuminating a display having a plurality of pixels, where each pixel contains a circuit for controlling application of energy to a light element, where said circuit comprises a drive transistor, said method comprising the steps of:

(a) determining an auto zero voltage for the drive transistor by applying a reference voltage on a data line;

(b) loading data onto the pixel by switching said reference voltage to a data voltage on said data line,

(c) storing said data on a capacitor that is coupled to the drive transistor; and

(d) illuminating said light element in accordance with said stored data.

9. A circuit (300) for driving a light element having two terminals, said circuit comprising:

a first transistor (360) having a gate, a source and a drain, where said gate is for coupling to a select line (320), where said source is for coupling to a data line (310);

a first capacitor (350) having a first terminal and a second terminal, where said drain of said first transistor is coupled to said first terminal of said first capacitor;

a second transistor (365) having a gate, a source and a drain, where said source of said second transistor is for coupling to a V_{DD} line (390), where said gate of said second transistor is coupled to said second terminal of said first capacitor;

a second capacitor (355) having a first terminal and a second terminal, where said gate of said second transistor is coupled to said first terminal of said second capacitor, where said source of said second transistor is coupled to said second terminal of said second capacitor;

a third transistor (370) having a gate, a source and a drain, where said gate of said third transistor is for coupling to an auto-zero line (330), where said source of said third transistor is coupled to said gate of said second transistor, where said drain of said third transistor is coupled to said drain of said second transistor; and

a fourth transistor (375) having a gate, a source and a drain, where said gate of said fourth transistor is for coupling to an illuminate line (340), where said source of said fourth transistor is coupled to said drain of said third transistor, where said drain of said fourth transistor is for coupling to the light element.

10. A system (500) comprising:

a display controller (510); and

a display (520), coupled to said display controller, where said display comprises a plurality of pixels, where each pixel (300) comprises:

a first transistor (360) having a gate, a source and a drain, where said gate is coupled to a select line (320), where said source is coupled to a data line (310);

a first capacitor (350) having a first terminal and a second terminal, where said drain of said first transistor is coupled to said first terminal of said first capacitor;

a second transistor (365) having a gate, a source and a drain, where said source of said second transistor is coupled to a V_{DD} line

(390) , where said gate of said second transistor is coupled to said second terminal of said first capacitor;

a second capacitor (355) having a first terminal and a second terminal, where said gate of said second transistor is coupled to said first terminal of said second capacitor, where said source of said second transistor is coupled to said second terminal of said second capacitor;

a third transistor (370) having a gate, a source and a drain, where said gate of said third transistor is coupled an auto-zero line (330) , where said source of said third transistor is coupled to said gate of said second transistor, where said drain of said third transistor is coupled to said drain of said second transistor;

a fourth transistor (375) having a gate, a source and a drain, where said gate of said fourth transistor is coupled to an illuminate line (340), where said source of said fourth transistor is coupled to said drain of said third transistor; and

a light element (380) having two terminals, where said drain of said fourth transistor is coupled to one of said terminal of said light element.

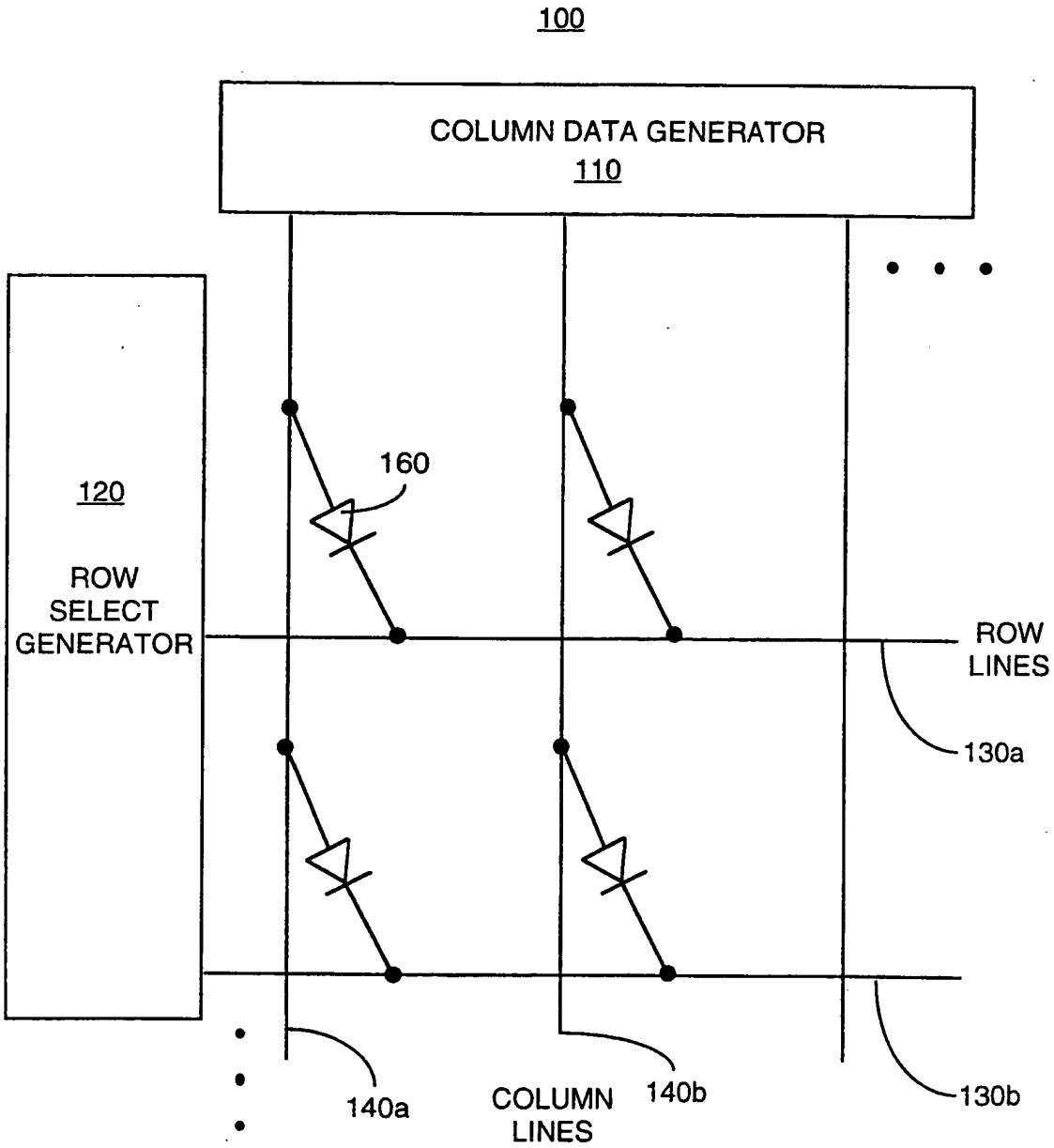
11. A display (520) comprising a plurality of pixels, each pixel (700) comprising:

a first transistor (710) having a gate, a source and a drain, where said gate is coupled to a select line (770) , where said source is coupled to a data line (760);

a second transistor (720) having a gate, a source and a drain, where said drain of said first transistor is coupled to said gate of said second transistor;

a resistor (750) having two terminals, where said source of said second transistor is coupled to one of said terminal of said resistor; and

a light element (740) having two terminals, where said drain of said second transistor is coupled to one of said terminal of said light element.



(PRIOR ART)

FIG. 1

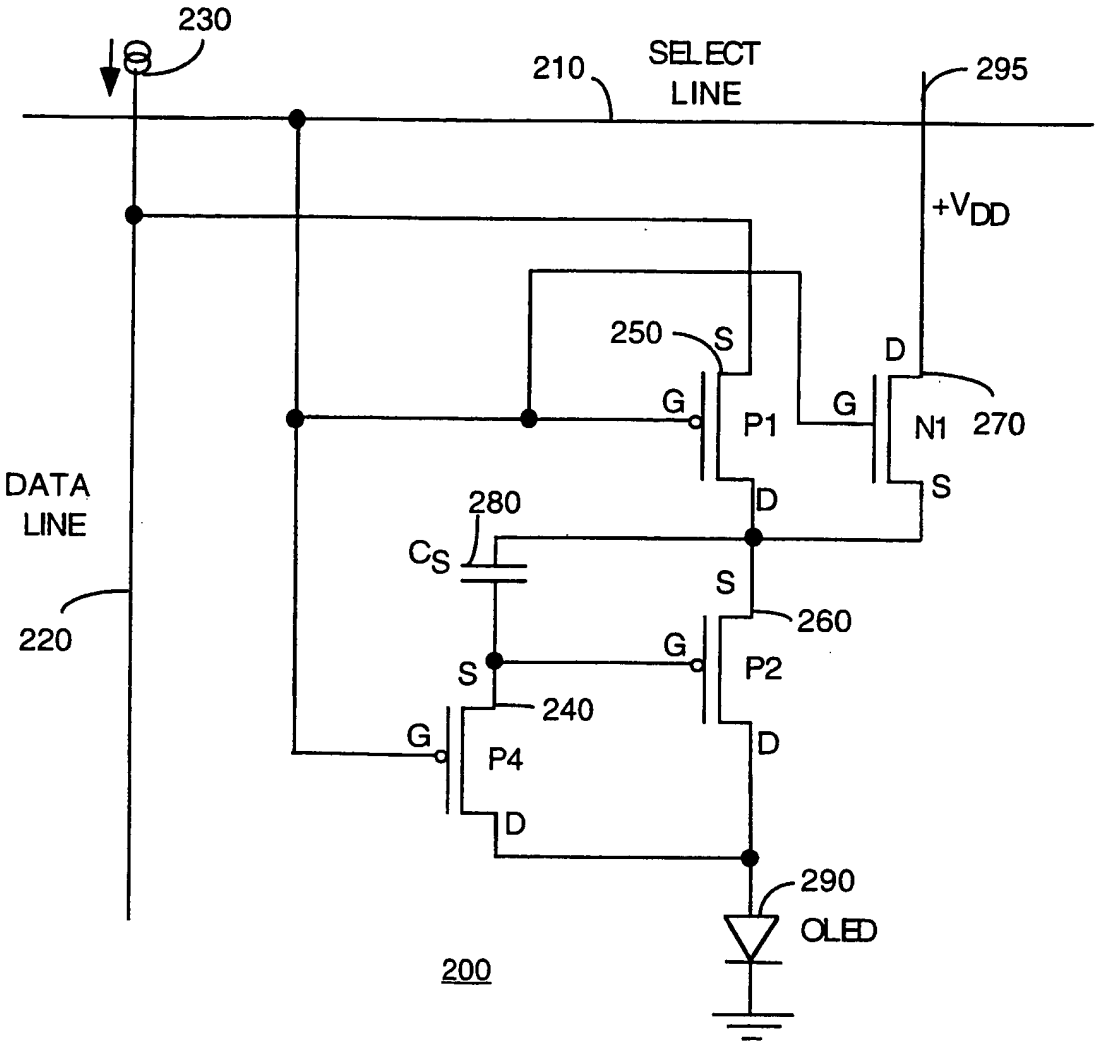


FIG. 2

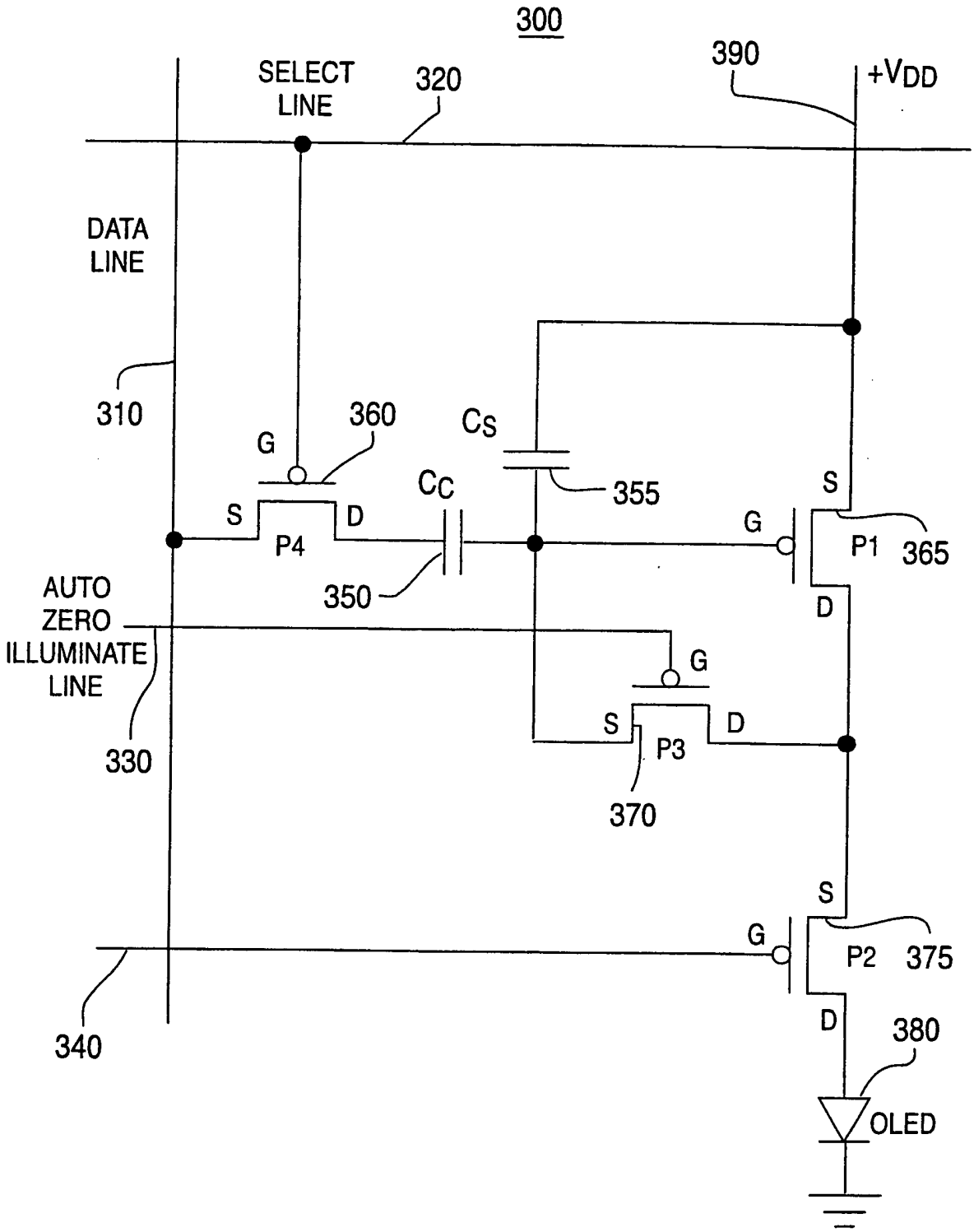

300
SELECT LINE
320
390
+VDD
DATA LINE
310
G
360
CS
355
CC
S
D
P4
350
G
S
P1
365
D
AUTO ZERO ILLUMINATE LINE
330
G
S
D
P3
370
S
G
P2
375
D
380
340
OLED

FIG. 3

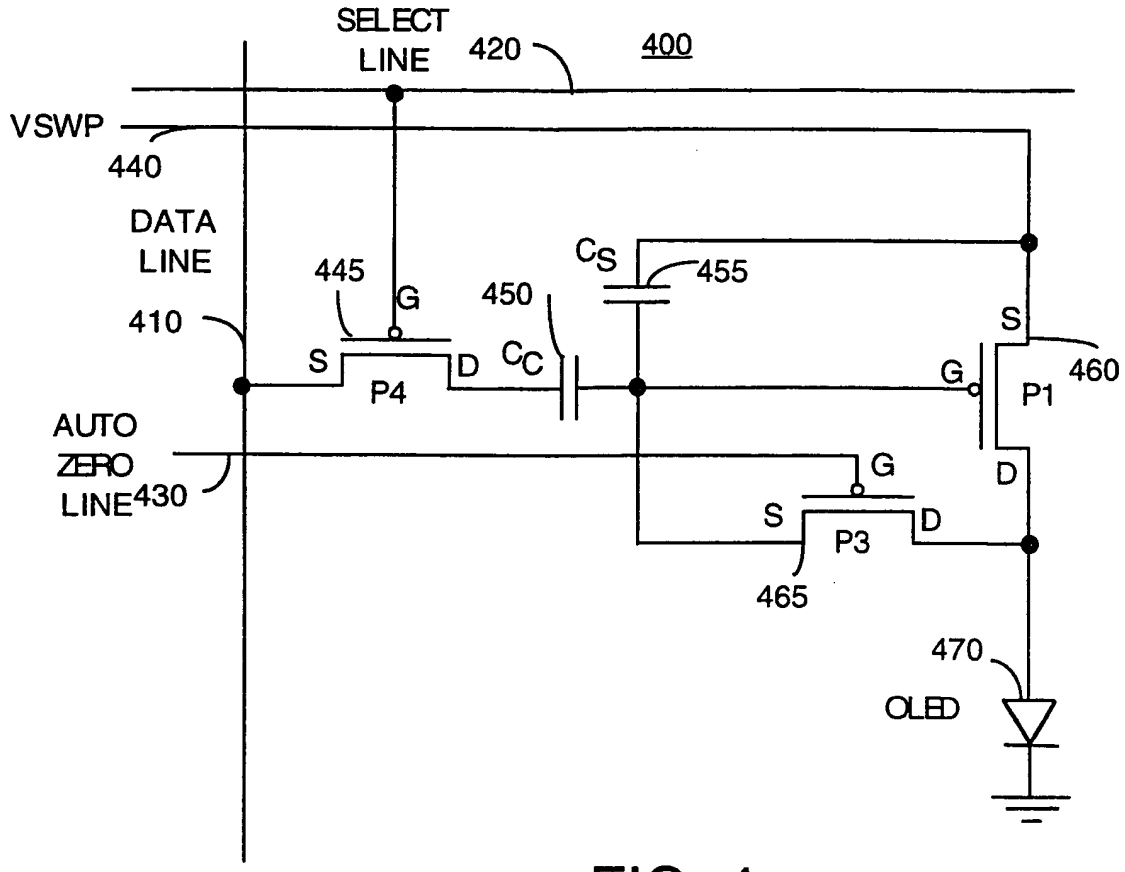


FIG. 4

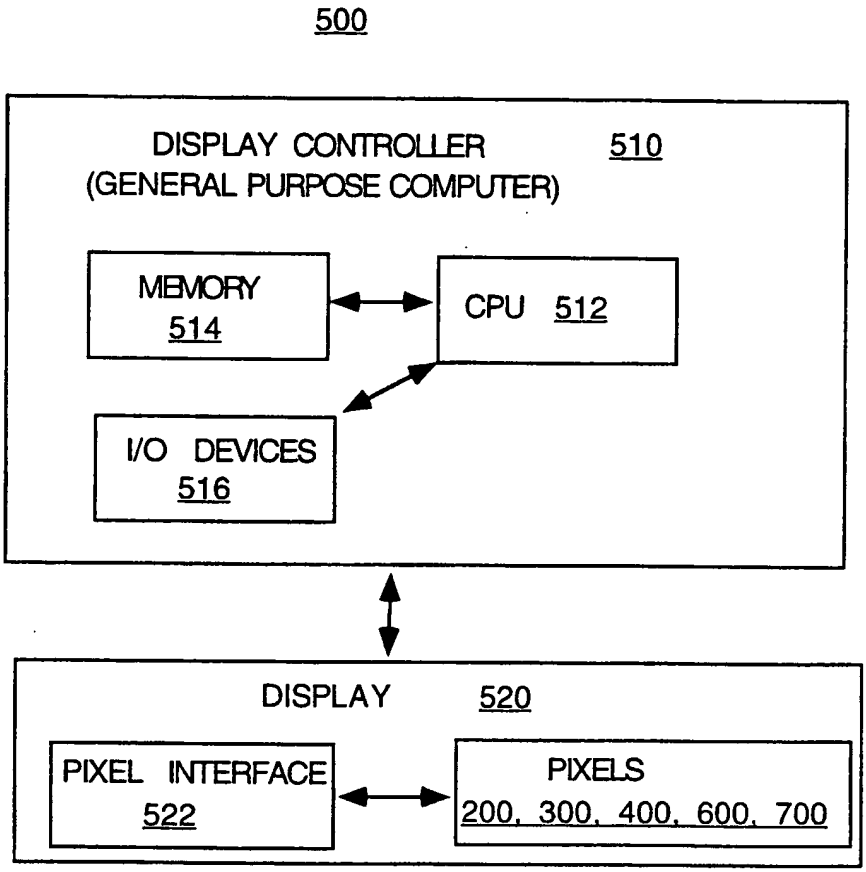


FIG. 5

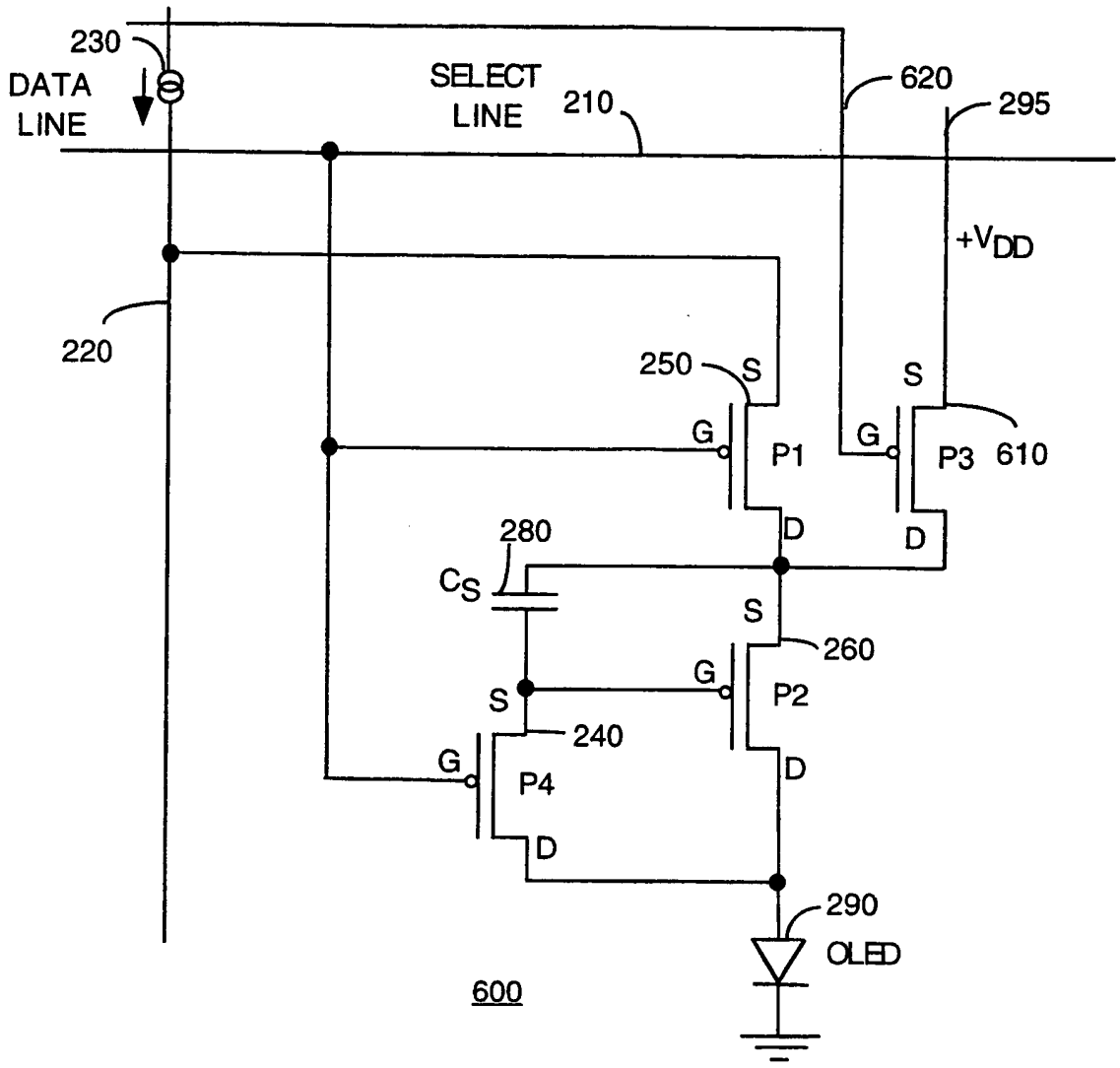

230
DATA LINE
SELECT LINE
210
620
295
+VDD
220
250
S
G
P1
G
P3
610
S
D
D
280
CS
S
260
G
P2
S
240
G
P4
D
D
290
OLED
600

FIG. 6

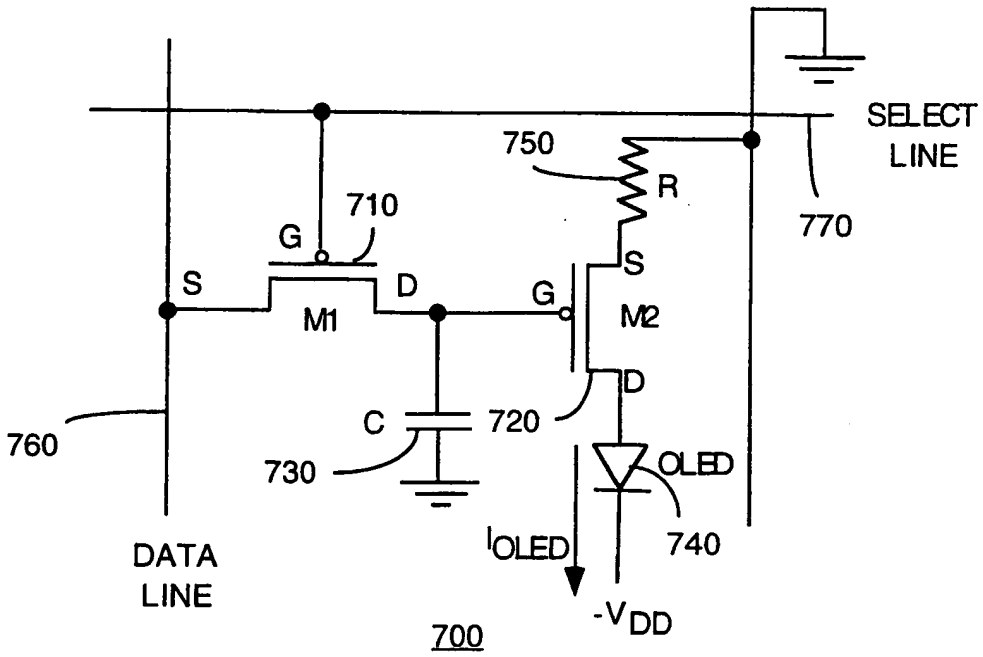

SELECT LINE
750
R
770
710
G
S
D
G
S
M1
M2
D
760
C
720
730
OLED
740
DATA LINE
IOLED
-VDD
700

FIG. 7

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US98/08367

A. CLASSIFICATION OF SUBJECT MATTER

IPC(6) :G09G 03/10
US CL : 315/169.3, 169.1; 345/76, 92
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 315/169.3, 169.1, 164, 160; 345/76, 92, 77, 147

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

NONE

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

NONE

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 5,302,966 A (STEWART) 12 April 1994 (12/04/94), see figures 2 and 4.	11
A	US 5,463,279 A (KHORMAEI) 31 October 1995 (31/10/95), see entire document.	1-11
A, P	US 5,684,365 A (TANG ET AL) 04 November 97 (04.11.97) see entire document.	1-11
X	US 5,095,248 A (SATO) 10 March 1992 (10/03/92), see figure 4.	11

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

*	Special categories of cited documents:	"T"	later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"A"	document defining the general state of the art which is not considered to be of particular relevance	"X"	document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"E"	earlier document published on or after the international filing date	"Y"	document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"L"	document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"&"	document member of the same patent family
"O"	document referring to an oral disclosure, use, exhibition or other means		
"P"	document published prior to the international filing date but later than the priority date claimed		

Date of the actual completion of the international search	Date of mailing of the international search report
16 JUNE 1998	31 AUG 1998
Name and mailing address of the ISA/US Commissioner of Patents and Trademarks Box PCT Washington, D.C. 20231 Facsimile No. (703) 305-7724	Authorized officer for HAISSA PHILOGENE Telephone No. (703) 305-3485

Form PCT/ISA/210 (second sheet)(July 1992)*